Amendments to the Specification:

Please replace the paragraph beginning at line 21 on page 13 with the following amended paragraph:

Figure 12 is a block diagram of a bus architecture for an embedded logic portion of a programmable logic device that includes dual port memory consistent with embodiments of the present invention. The memories are shown as SRAMs, but, as with all the memories shown in the included figures, they can be other memory types, such as DRAM, Flash, EPROM, EEPROM, or any other memory type. Processor 1208 has a dedicated bus, AHB1 1210, which gives the processor access to interrupt controller 1204, watchdog timer 1206, test interface controller 1212, memory controller 1218, single port SRAMs 1226 and 1228, and dual-port SRAMs 1232 and 1234. An example of a watchdog timer 1206 can be found in commonly-assigned patent application number [[_____]] 09/880734, filed on June 12, 2001, attorney docket number 15114-53500US, incorporated by reference for all purposes. Processor 1208 may access a second bus, AHB2 1220, through the AHB1-2 bridge 1224. Coupled to the AHB2 bus 1220 are a universal asynchronous receiver and transceiver (UART) 1214, a bus expansion block 1216, timer 1236, reset load controller 1238, configuration logic 1242, PLD Master and slave bridges 1248 and 1244, as well as memory controller 1218, clock generators 1222, the single port SRAMs 1226 and 1228, and dual-port SRAMs 1232 and 1234. The dual-port SRAMs 1232 and 1234 interface to the programmable logic portion 1202, and in an embodiment, to a shared input/output structure. In an embodiment of the present invention, both buses AHB1 1210 and AHB2 1220 are 32 bits wide. Alternately, they may be other widths, and they may be of unequal widths. For example, they may be 16, or 64, or 128 bits wide.